ABSTRACT OF THE DISCLOSURE

An object of the invention is to provide a bit synchronizing circuit of high quality comprising a bit synchronizing circuit used in a reception circuit for serial communication having a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a substantially regular interval, based on an input clock and a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock.